Design and Performance of Clock-Recovery GaAs ICs for High-Speed Optical Communication Systems

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***Abstract*—Design and performance of clock-recovery GaAs ICs are presented. Four kinds of ICs were developed: a limiting amplifier, a tuning amplifier, a rectifier, and a differentiator. The cascaded limiting amplifier together with a tuning amplifier achieved a 58-dB gain and a 10-degree phase deviation with 20-dB input dynamic range at 10 GHz. A clock-recovery circuit successfully extracts a low-jitter 10-GHz clock signal of 1-dBm constant power from 10-Gb/s NRZ pseudorandom bit streams using a pulse pattern generator.**

I. Introduction

RECENTLY, optical communication systems operating at 10 Gb/s data rates are attracting considerable interest for high-capacity communication systems [1]. A key component to realize such systems is a high-speed clock recovery circuit. Monolithic integration is also required to achieve compact and low-cost systems that offer fail-safe reliability. Several high-speed clock-recovery ICs have been developed using GaAs MESFETs and heterostructure devices [2]–[4]. GaAs ICs are clearly the most realistic candidates to realize the systems considering the maturity of this material system and device technology. GaAs IC technologies have already been applied to 10-Gb/s data-recovery circuits and they have demonstrated excellent performance. [5]–[7]. A key design issue for clock-recovery circuits is how to reduce phase deviation over a wide dynamic range in a limiting amplifier because this has a great impact on recovered-lock phase deviation and jitter.

This paper describes design techniques and performance of GaAs clock-recovery ICs for high-speed optical communication systems. Four kinds of IC are covered: a limiting amplifier, a tuning amplifier, a rectifier, and a differentiator. A noteworthy feature of the limiting-amplifier design is that it suppresses spurious harmonic signals to reduce phase deviation. The other ICs feature a tuning amplifier with a voltage-controlled tuning frequency, a Gilbert-cell-based rectifier, and a differentiator with an on-chip $\lambda/4$ coplanar-waveguide short stub, respectively.

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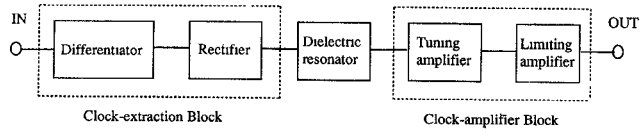


Fig. 1. Block diagram of clock-recovery circuit.

II. Circuit Design

A block diagram of the clock-recovery circuit is shown in Fig. 1. It consists of a differentiator IC, a rectifier IC, a dielectric resonator, a tuning amplifier IC, and limiting amplifier ICs. The differentiator and rectifier extract a clock signal from a data signal. A high-Q dielectric resonator is used for a timing tank. A tuning amplifier acts as an active band-pass filter to suppress the jitter caused by the high-order mode of the dielectric resonator [4]. Limiting amplifier ICs were cascaded to obtain a high gain of 60 dB. Circuit simulation was performed using an FET model with an ft of 40 GHz and an fmax of 70 GHz

1. Limiting Amplifier

Because a clock's amplitude from a dielectric resonator is strongly modulated by a data pattern, a limiting amplifier is required to maintain low phase deviation over a wide input dynamic range to provide an aligned clock for a decision circuit. In previous studies [8], [9], emphasis was placed on minimizing the signal phase delay as a way to reduce the phase deviation. In these studies, the circuit was simplified to avoid additional phase delay or the pole frequency was increased to reduce phase delay at the operating frequency. In this paper we will concentrate on the effects spurious harmonics have on phase deviation.

A limiting amplifier operates under highly non-linear conditions when it limits the output power. High-order harmonics are generated in the limiting operation and they also have phase deviation. The harmonics thus affect the phase deviation of the total output waveform. A schematic illustrating the effect when a second harmonic is dominant is shown in Fig. 2. Phase deviation is defined as the variation in input-to-output signal phase shift to the input power variation. Since the phase deviation is very small in any linear region, we can redefine phase deviation in Fig. 2 for convenience to refer specifically to the phase shift from an output signal in a linear region to that in a limiting region. Here, $\theta 21$ and $\theta 22$ are the phase deviations of output fundamental and second-harmonic

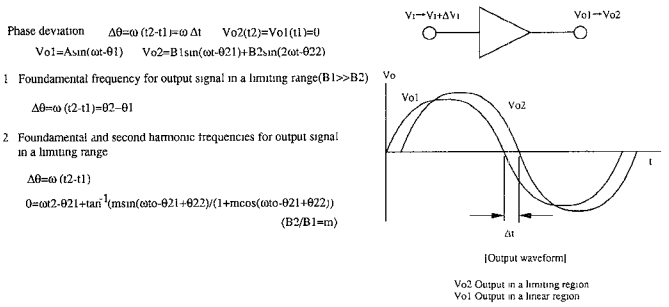


Fig. 2. Effect of second harmonic on phase deviation.

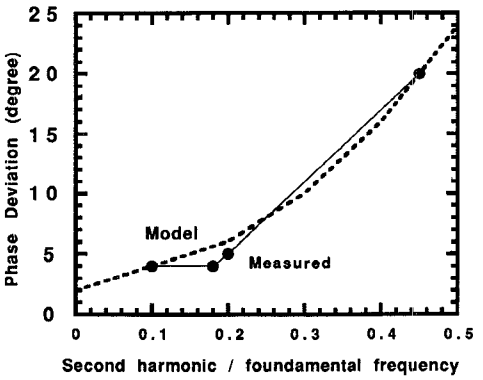


Fig. 3. Phase deviation versus ratio of fundamental frequency to second harmonic. Solid line: Experimental results. Dashed line: Calculated results.

frequencies. They are affected by the powers of the input signal and generated second harmonics, respectively, due to the nonlinear bias dependence of the transistor capacitances. When a second harmonic is not negligible in a limiting region, the phase deviation of the total waveform is related to that of the second harmonic ($\theta 22$) as illustrated in the simple analytical formula shown in Fig. 2. Phase deviation increases as $\theta 22$ or/and the ratio of the fundamental to the second harmonic frequency (m) increase.

Experimental results respecting the second harmonic effect on the phase deviation are shown in Fig. 3. The phase deviation is plotted a function of the amplitude ratio of the output fundamental frequency to the output second harmonic. For this experiment, the suppression of the second harmonic was varied using different-frequency-band amplifier ICs with the same 10-GHz gain, structure and transistors combined with an external filter. Frequency and dynamic range of the input signal were 10 GHz and 15 dB. Phase deviation was measured using a sampling oscilloscope with 40-GHz sampling head. It was found that the phase deviation fell off sharply as the second harmonic decreased. Calculated results using the analytical formula with $\theta 21$ and $\theta 22$ as fitting parameters are also shown in Fig. 3. We assume that $\theta 22$ varies inversely with the second-harmonic amplitude. While it is very difficult to specify the cause of $\theta 21$ and $\theta 22$ in quantitative forms, it is nevertheless apparent that the simple analytical model explains the experimental results quite well.

As the above results make clear, suppression of the second harmonic is very effective for reducing the phase deviation

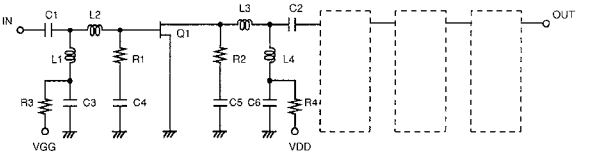


Fig. 4. Schematic of limiting amplifier.

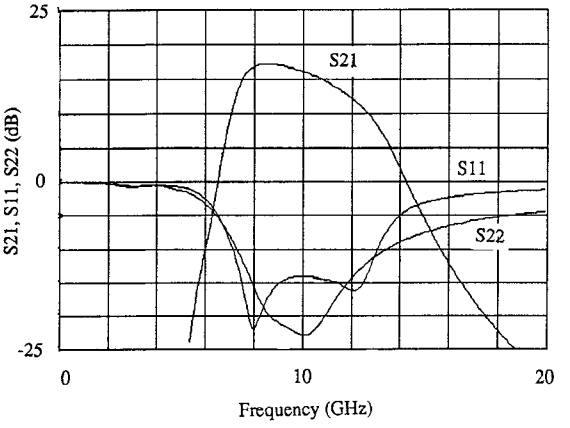


Fig. 5. Simulated results for limiting amplifier. (a) frequency dependencies of $S21$, $S11$, and $S22$. (b) Output waveforms for input powers of -10, 0, 5, 10 dBm.

of a limiting amplifier. In actual circuits, a differential configuration [2] or a narrow-band configuration which suppresses second harmonic frequency is suited to suppress the second harmonic because of its simplicity. In the present design, a narrow-band configuration was chosen because it is also capable of easily deriving a high gain at microwave frequencies thanks to inherent high-fmax performance of GaAs MESFETs. Note that this is a completely different approach than tried in previous studies because almost all limiting amplifiers for optical communication systems have employed wideband configurations [2], [3], [8], [9]. A schematic circuit of the limiting amplifier is shown in Fig. 4. It has a 4-stage construction with input, output and interstage impedance-matching networks. The gate width of FET is 100 μm. The multi-stage construction was used to reduce the peak gate-to-drain voltage applied to each FET during a limiting operation. Simulated results are presented

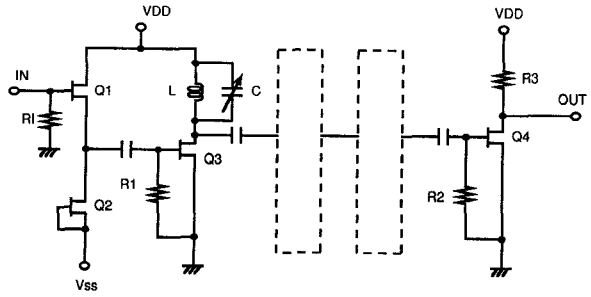


Fig. 6. Schematic of tuning amplifier.

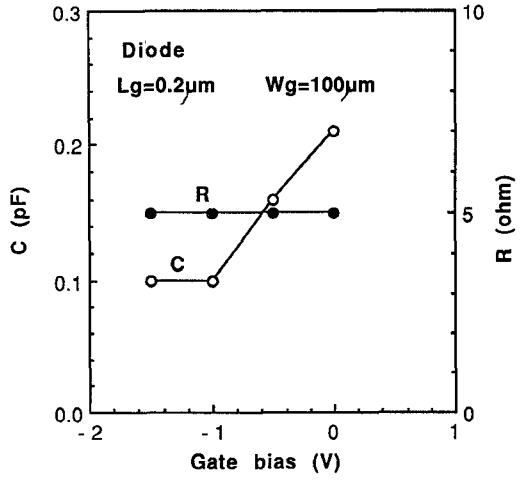


Fig. 7. Bias dependencies of capacitance and resistance for diode.

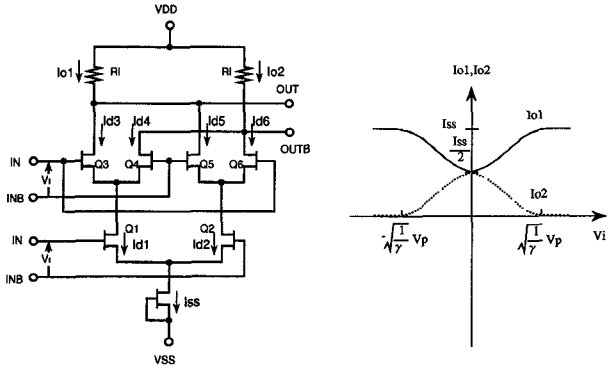


Fig. 8. Schematic for Gilbert cell and transfer characteristic.

TABLE I
TRANSFER CHARACTERISTIC OF GILBERT CELL

Io1	$\frac{Iss}{2}\left(1+\left(\frac{Vi}{Vp}\right)^2\left(2\gamma-\gamma^2\left(\frac{Vi}{Vp}\right)^2\right)\right)$
Gc	$2K\frac{Vi}{Vp}\left(2-\left(\frac{Vi}{Vp}\right)^2\right)$
$\left(\frac{Idi}{(i=1,2)}\right)$	$K(Vgs-Vp)^2=Idss\left(1-\frac{Vgs}{Vp}\right)^2$
$\left(\frac{Idi}{(i=3\sim6)}\right)$	$K'(Vgs-Vp)^2=Idss'\left(1-\frac{Vgs}{Vp}\right)^2$
γ	$\frac{Idss}{Iss}=\frac{Idss'}{Idss}$
Gc	$\frac{\partial Io1}{\partial Vi}$

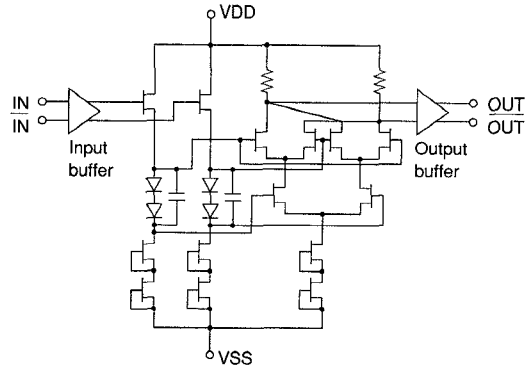


Fig. 9. Schematic of rectifier.

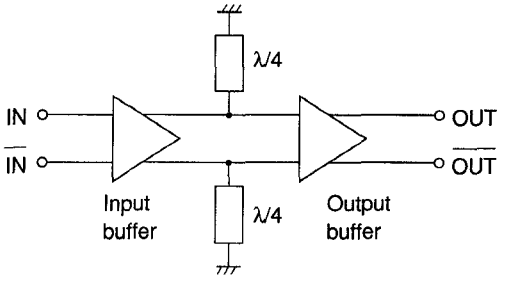
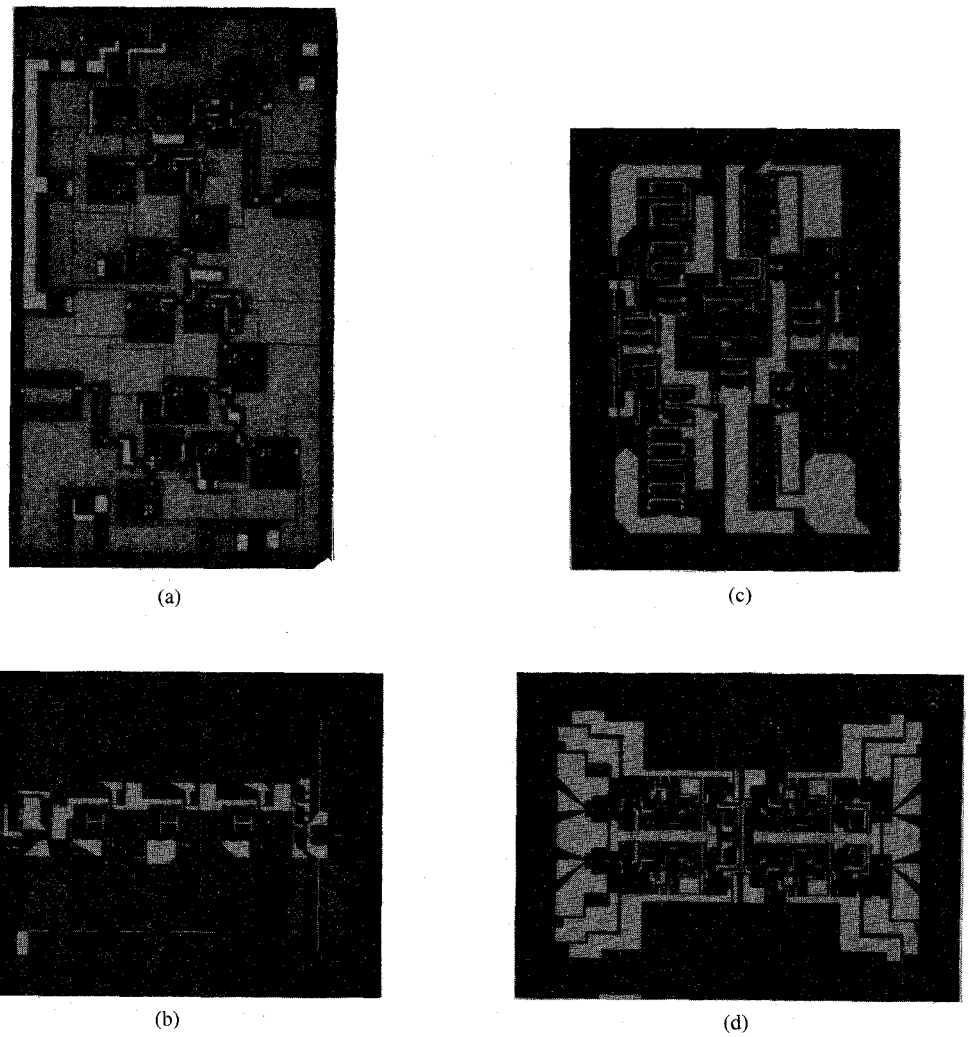


Fig. 10. Schematic of differentiator.

in Fig. 5. They were simulated using a modified MESFET model based on hyperbolic tangent Ids-Vds relation [8]. Bias dependencies of equivalent-circuit parameters were extracted by fitting the measured S parameters. Simulated results include extrinsic effects of bonding-wire inductances. Four output waveforms for input powers of -10, 0, 5, 10 dBm are traced in Fig. 5. The amplifier was designed to yield a gain of more than 15 dB with $S11$ and $S22$ less than -14 dB at 10 GHz. Simulated output signals reveal very small phase deviation up to an input power of 10 dBm.

2. *Tuning Amplifier*

An LC parallel-resonance circuit was employed for a tuning amplifier. A schematic circuit is shown in Fig. 6. It consists of a common-source FET with an LC resonance circuit on the drain side. A small gate width of 25 μm was used to increase the FET output resistance parallel to the LC resonance circuit. Three tuning stages were cascaded to increase the gain and Q factor at the tuning frequency. For the inductance, a monolithic spiral inductor of 1 nH with 2-Ω series resistance was employed. The tuning frequency was voltage-controlled using the variable capacitance of a diode. Bias dependencies of the capacitance and series resistance are shown in Fig. 7. The diode employs the same structure as that of a MESFET with ion-implanted channel and n^+ layers. Impedance matchings



(a) (c)

(b) (d)

Fig. 11. Microphotographs of ICs. (a) Limiting amplifier. (b) Tuning amplifier. (c) Rectifier. (d) Differentiator.

were obtained in a wide frequency band with source-follower and common-source FETs as buffers. The gain was designed to be 10 dB at a tuning frequency of 10 GHz with gain reduction of about 20 dB at frequencies 2-GHz removed from the tuning frequency. A tuning frequency was changed by about 2 GHz using the controlled bias.

3. *Rectifier*

A Gilbert cell [10] operates as either doubler or full wave rectifier when the signals with the same frequency or shape are applied at two differential input ports. A schematic Gilbert cell circuit and transfer characteristics are shown in Fig. 8. The analytical expressions of the transfer characteristics are also shown in Table I. The transfer characteristic was derived using a cubic I-V formula for MESFETs with a threshold voltage Vp. A Gilbert cell operates as a doubler with small spurious output signals when the input signal Vi is small enough compared with Vp to neglect high-order terms of Vi/Vp. For relatively large input signals, it operates as a full wave rectifier because of the symmetric transfer characteristic. Since spurious output signals were rejected by the next-stage dielectric resonator used for the clock-recovery circuit, the Gilbert-cell was designed to operate as a full wave rectifier for this work. Fig. 9 shows a schematic of the entire circuit. A differential amplifier was used as an active balun for an input buffer. Input signals were split in-phase and applied at Gilbert-cell input ports by level-shifters. Input and output buffers also provided good impedance matchings over a wide frequency range.

4. *Differentiator*

A schematic differentiator circuit is shown in Fig. 10. A $\lambda/4$ short stub was employed to different signals. Compared with an RC differentiator, a $\lambda/4$ differentiator is less affected by fabrication parameter variations. The short stub was monolithically integrated using a compact meandering coplanar waveguide.

III. Fabrication

ICs were fabricated using advanced self-aligned implantation for n^+ layer technology (ASAINT) [11]. The gate length and threshold voltage were 0.2 μm, and -0.8 V. The ft and fmax of the MESFETs were 40 GHz and 70 GHz, respectively. Microphotographs of the ICs are shown in Fig. 11. Chip sizes were 1.5×2.5 mm for the limiting amplifier, 2×1.5 mm for

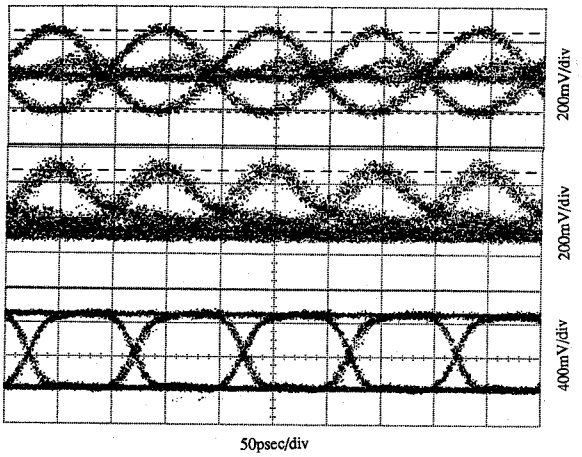


Fig. 12. Waveform characteristics of clock-extraction block for 10-Gb/s NRZ PRBS signal. (a) Output waveform of differentiator. (b) Output waveform of clock-extraction block. (c) Monitored waveform for inverting input data.

the tuning amplifier, 1.5 × 2 mm for the rectifier, and 2 × 1.5 mm for the differentiator. After all ICs were subjected to on-wafer testing, they were encased in metal-based packages [6]. The package has a cavity size of 6 × 3.5 mm with coplanar-waveguide signal lines. The isolation was more than 50 dB at 10 GHz.

IV. Performance

1. Clock-Extraction Block

Packaged differentiator and rectifier ICs were cascaded to construct a clock-extraction block (Fig. 1). OUT and OUT nodes of the differentiator were dc-connected to IN and IN nodes of the rectifiers. Input data and a reference voltage were applied to IN and IN ports of the rectifier, respectively. Supply voltages were 5 V and −3 V with a total power consumption of about 1.2 W. Fig. 12 shows output waveforms of the differentiator and clock-extraction block for input data of 10 Gb/s NRZ $2^{23} - 1$ pseudorandom bit streams (PRBS) from a pattern generator. High and low levels of input data were 0 V and −0.9 V. Monitored input inverting data are also shown in Fig. 12. The ICs operated very well up to the speeds of 10 Gb/s. The output waveform of the differentiator showed a slight ripple. This is because of the 50 Ω termination of the $\lambda/4$ short stub was not perfect, giving rise to a reflection. A differentiator output for 5-Gb/s NRZ input signal is also shown in Fig. 13 to illustrate the function of a $\lambda/4$ short stub. A pulse train with about 50-psec pulse width and 200-psec period was generated by the differentiator. The pulse width corresponds to $\lambda/2$ at 10 GHz. The mark-density dependencies of the extracted clock-signal power are shown in Fig. 14. Clock signal powers of −20 to −34 dBm were extracted over a mark-density range from 1/8 to 7/8.

2. Clock-Amplifier Block

One packaged tuning amplifier and four packaged limiting amplifier ICs were cascaded to produce clock-amplifier block (Fig. 1). Supply voltages were 1 V and −3 V with a total power consumption of 130 mW. Frequency dependencies of

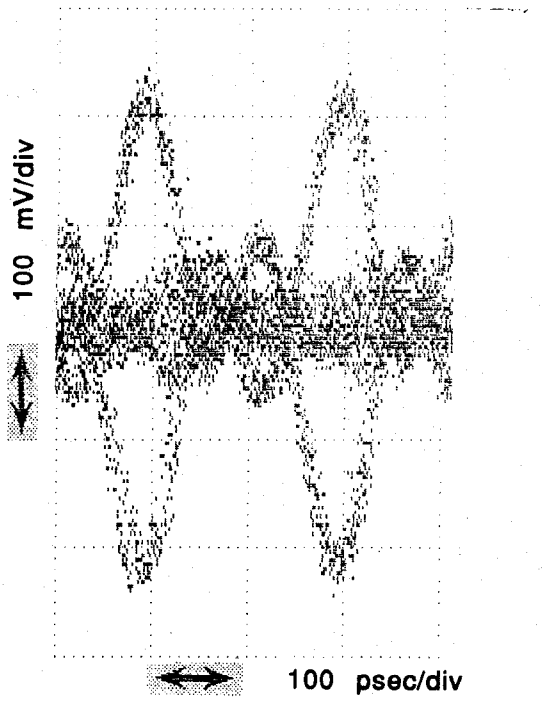


Fig. 13. Output waveform of differentiator for 5-Gb/s NRZ PRBS signal.

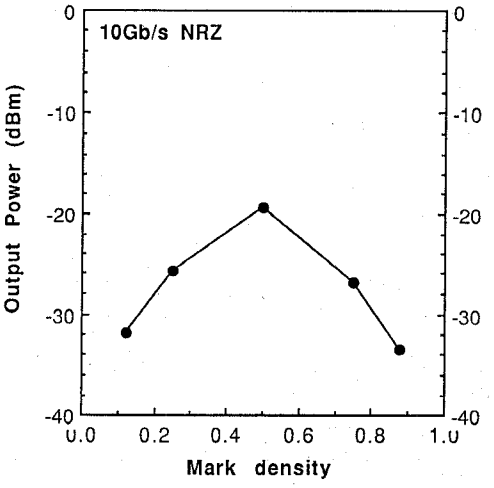


Fig. 14. Mark-density dependencies of extracted clock-signal power.

$S21$, $S11$ and $S22$ for the amplifier block are shown in Fig. 15. The amplifier had a high gain of 58 dB with $S11$ and $S22$ of less than −20 dB at 10 GHz. Good bandpass performance was obtained with a gain reduction of more than 15 dB at 8 and 12 GHz. The gain reduction was well enough to suppress the increase in jitter due to high-order modes of the dielectric resonator. $S21$ peaked at 9.5 GHz because the tuning frequency of the tuning amplifier shifted beyond the variable-frequency range and couldn't be adjusted by the control bias. It is because the tuning frequency was affected by the extrinsic inductances of IC patterns and bonding wires more than expected in the design. The input-power dependencies of output power and phase deviation are shown in Fig. 16. The amplifier achieved a small phase deviation of less than 10 degrees with a saturated power of 1 dBm in the input dynamic range from −55 dBm to −35 dBm.

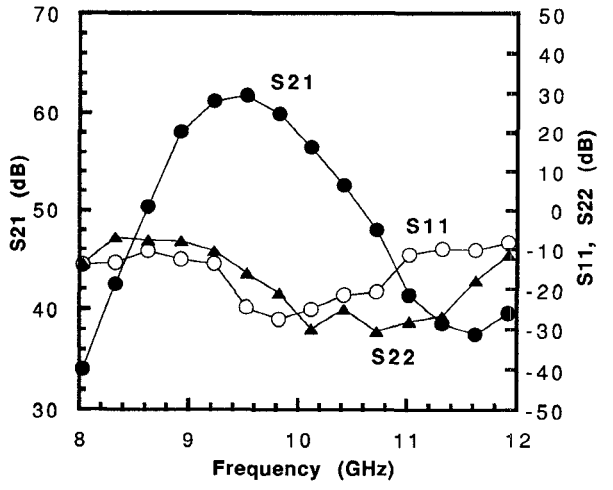


Fig. 15. Frequency dependencies of $S21$, $S11$ and $S22$ for clock-amplifier block.

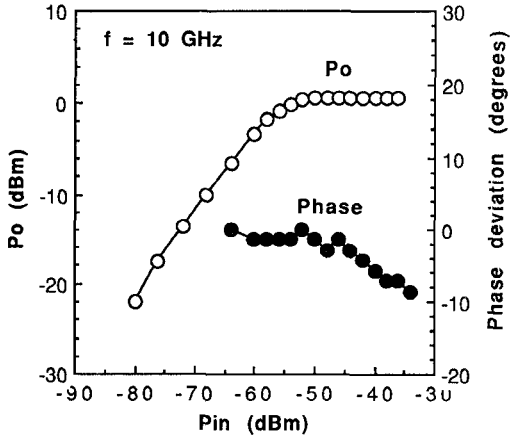


Fig. 16. Output power and phase deviation versus input power for clock-amplifier block.

3. Clock-Recovery Circuit

The clock-recovery circuit shown in Fig. 1 was tested using the clock-extraction and amplifier blocks. The dielectric resonator had about 6-db loss at 10 GHz with a Q factor of about 1000. Attenuators were inserted into the circuit to adjust the power level. Fig. 17 shows the frequency spectrum of an output signal for input data of 10 Gb/s NRZ $2^{23}-1$ PRBS from a pattern generator. RMS jitter of the recovered clock signal was 1.4 degrees at a mark density of $1/2$ and was maintained within 2.5 degrees in the mark-density range centering on $1/2$ from $1/8$ to $7/8$.

V. Conclusion

Design techniques and performance of GaAs clock-recovery ICs for application to high-speed optical communication systems were described. The key feature of the limiting-amplifier design that we highlight in this paper is that spurious harmonic signals are suppressed to reduce phase deviation. Noteworthy features of the other ICs were a tuning amplifier with a voltage-controlled tuning frequency, a Gilbert-cell-based rectifier, and a differentiator with an on-chip $\lambda/4$ coplanar-waveguide short stub, respectively. Combining these techniques, a 10-Gb/s GaAs clock-recovery circuit was successfully developed. Considering their overall performance-high speed, high gain, and small size—these devices should have a considerable impact on high-speed optical communication systems.

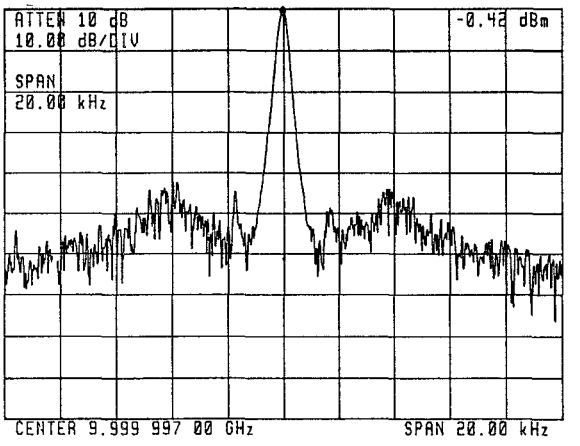


Fig. 17. Frequency spectrum of recovered clock signal for clock-recovery circuit.

Acknowledgment

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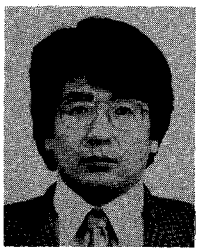

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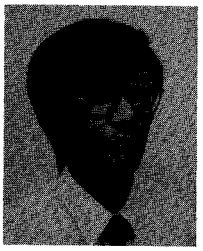

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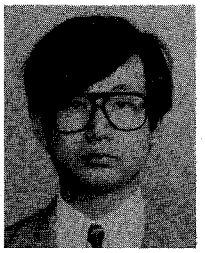

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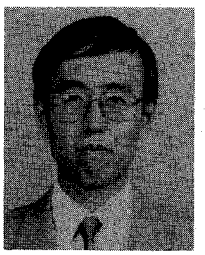
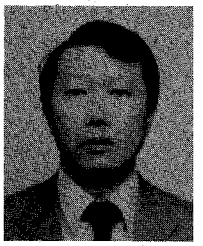


Noboru Ishihara (M'89) was born in Gunma, Japan, on April 27, 1958. He received his B.S. degree in electrical engineering from Gunma University, Gunma, Japan, in 1981.

In 1981, he joined the Electrical Communication Laboratory, NTT, Tokyo, Japan, where he has been engaged in research and development of high-speed analog IC's for communication use. His recent work is in the area of low-power and high-speed analog IC's.

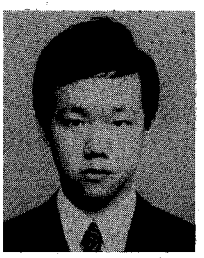
Mr. Ishihara is a member of the Institute of Electronics, Information and Communication Engineers of Japan.



Hiroyuki Kikuchi (M'89) was born in Tokyo, Japan, on April 28, 1948. He received the B.S. and M.S. degrees in electronic engineering from Keio University, Kanagawa, Japan, in 1972 and 1974, respectively.

In 1974 he joined NTT Electrical Communication Laboratory, Tokyo, Japan. He initially did research and development work on CMOS digital and analog LSI's for communication use. He also worked in high-frequency analog IC's for satellite and optical communication systems. In 1989 he was transferred to the NTT Electronics Technology Corporation, Tokyo, Japan, where he is involved in the development of broadband GaAs analog IC's.

Mr. Kikuchi is a member of the Institute of Electronics, Information and Communication Engineers of Japan and the IEEE Microwave Theory and Techniques Society.



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In 1987, he joined NTT Transmission Systems Laboratories, Yokosuka, Kanagawa, Japan, where he has been engaged in research on high-speed optical communication systems. His current research interests include high-speed semiconductor devices.

Mr. Ono is a member of the Institute of Electronics, Information, and Communications Engineers of Japan.